We claim:

1. A semiconductor device comprising:

at least first and second levels of interconnect conductor for connection to a semiconductor layer; and

a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane and formed between the first and second levels of conductor, including

a first conductive layer,

a first insulator layer formed over the first conductive layer,

a second conductive layer formed over the first insulative layer ,

a second insulator layer formed over the second conductive layer, and

a third conductive layer formed over the second insulative layer,

with the first and third conductive layers commonly connected.

2. The device of claim 1 wherein the first and third conductive layers are commonly connected through the first and second levels of interconnect conductor.

3. The device of claim 1 further including a third level of interconnect conductor with the first and second conductor layers commonly connected through the first, second and third levels of interconnect conductor.

4. The device of claim 1 wherein the conductors connecting the first and third conductive layers include via portions and trench portions of a Damascene structure.

5. The device of claim 1 wherein the stack of alternating conductive and insulative layers includes one or more pairs of additional conductive and insulative layers formed

over the third conductive layer providing an uppermost conductive layer commonly connected with the first and third conductive layers.

6. The device of claim 5 wherein the stack comprises 5 conductive layers configured to provide 4 capacitors connected in parallel.

7. A method for making a semiconductor device with a capacitor structure, comprising:

providing a first insulative layer;

forming a first conductive runner on the first insulative layer;

forming a second conductive runner above the first conductive runner;

forming a stack of alternating conductor and dielectric layers between the first conductive runner and the second conductive runner; and

etching an opening in an upper most of the conductive layers and extending the opening through an adjoining dielectric layer to a first underlying conductor layer.

8. The method of claim 7 further including the step of connecting the upper most of the conductive layers with a conductor layer below the first underlying conductor layer.

9. The method of claim 8 wherein the stack is formed by depositing first, second and third conductor layers and the step of connecting the uppermost conductor layer includes connecting the first conductor layer to the third conductor layer.

10. The method of claim 8 wherein the stack is formed by sequentially depositing first, second, third, fourth and fifth conductor layers separated from one another by intervening dielectric layers and the step of connecting the upper most layer includes connecting the first, third and fifth layers in common.